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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,747	11/20/2003	Richard James Eickemeyer	ROC920020128US1	8785

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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,747	EICKEMEYER ET AL.	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-22 have been examined.

Acknowledgment of papers filed: oath, specification, drawings, and IDS, on November 20th, 2003. The papers filed have been placed on record.

Specification

2. The title is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 and 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Doing (U.S. Patent No. 6,348,671).

5. Regarding claim 1, Doing discloses an integrated circuit processor (col 2 lines 52-53) comprising: a first instruction buffer (fig 2 reference 203) corresponding to a primary thread (col 7 lines 55-56); a second instruction buffer (fig 2 reference 204) corresponding to a backup thread (col 7 lines 60-64); a thread switch mechanism that detects when the primary thread stalls (col 14 lines 21-27), and in response thereto,

swaps information stored in the first instruction buffer with information stored in the second instruction buffer (col 7 line 52 to col 8 line 3).

Note that the sequential buffer holds instructions ment for the current thread and the thread switch buffer holds instructions in case of a thread switch. Clearly, this would indicate that after a context switch, the instruction contents of these registers would be swapped, much other thread-related information (ie col 14 lines 4-9 and col col 11 lines 51-62).

6. Regarding claim 2, Doing discloses the integrated circuit processor of claim 1 wherein execution of the backup thread occurs after the swap by executing at least one instruction in the first instruction buffer (col 7 line 52 to col 8 line 3).

Note that, after the instructions have been swapped, the backup instructions (considered to be "execution of the backup thread") are executed by collecting these instructions from the sequential buffer (also known as the "first instruction buffer").

7. Regarding claim 9, Doing discloses a method for switching between a first thread of execution and a second thread of execution in a multithreaded processor (col 7 line 52 to col 8 line 3), the method comprising the steps of: (A) providing a first instruction buffer (fig 2 reference 203) corresponding to the first thread (col 7 lines 55-56); (B) providing a second instruction buffer corresponding to the second thread (fig 2 reference 204 and col 7 lines 60-64); (C) swapping information stored in the first

instruction buffer with information stored in the second instruction buffer (col 7 line 52 to col 8 line 3).

8. Regarding claim 10, Doing discloses the method of claim 9 wherein step (C) is performed when switching between the first thread and the second thread is required (col 7 lines 60-64).

9. Regarding claim 11, Doing discloses the method of claim 9 wherein step (C) is performed when the first thread stalls (col 14 lines 21-27).

10. Regarding claim 12, Doing discloses the method of claim 9 wherein step (C) is performed when the second thread stalls (col 14 lines 21-27).

Note that the thread mechanisms are considered to be symmetric. See claim 8.

11. Regarding claim 13, Doing discloses the method of claim 9 further comprising the step of executing the second thread after the swapping of information in step (C) by executing at least one instruction in the first instruction buffer (col 7 line 52 to col 8 line 3).

See claim 2.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-6, 8, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing in view of Shoemaker (U.S. Publication No. 2003/0135711).

14. Regarding claim 3, Doing discloses the integrated circuit processor of claim 1.

Doing fails to disclose a third or fourth instruction buffer that swap instructions in a similar fashion as the first and second instruction buffer.

Shoemaker discloses the technique of Simultaneous Multi-Threading (paragraph 6).

It is expected that one of ordinary skill in the art would appreciate the fact that additional parallelism in a processing system allows for additional throughput. The technique of Simultaneous Multi-Threading is well known and has the advantages of allowing "multiple threads to share and to compete for processor resources at the same time". Doing, a processing system concerned with latency during stalls would be motivated to incorporate this technique to allow "the SMT system to continue executing useful work during a cache miss".

It would have been obvious at the time of the invention for one of ordinary skill in the art to add SMT capabilities (as in Shoemaker) to the computing system of Doing in

such a way that the primary and backup threads are replicated to create a "third" and "fourth" instruction buffer, also considered to be secondary primary and backup buffers.

Note that, logically, it would be obvious to simply replicate portions of the original invention of Doing to allow for SMT capabilities. For that reason, future references to third and forth buffers will be treated the same way as the first and second buffers, disclosed by Doing alone. Consequently, Doing/Shoemaker discloses the remaining limitations.

15. Regarding claim 4, Doing/Shoemaker discloses the integrated circuit processor of claim 3 wherein the first and second primary threads simultaneously issue instructions for execution (Shoemaker paragraph 6).

16. Regarding claim 5, Doing/Shoemaker discloses an integrated circuit processor (col 2 lines 52-53) comprising: a first primary instruction buffer (col 2 lines 52-53) corresponding to a first primary thread (fig 2 reference 203); a second primary instruction buffer corresponding to a second primary thread (see claim 3); wherein the first and second primary threads simultaneously issue instructions for execution (Shoemaker paragraph 6); a first backup instruction buffer (col 7 lines 55-56); a second backup instruction buffer; a thread switch mechanism that detects when one of the first and second threads stalls (col 14 lines 21-27), and in response thereto, swaps information stored in one of the first and second primary instruction buffers

corresponding to the stalled thread with information stored in one of the first and second backup instruction buffers (col 7 line 52 to col 8 line 3).

17. Regarding claim 6, Doing/Shoemaker discloses the integrated circuit processor of claim 5 wherein the thread switch mechanism: (1) detects when the first primary thread stalls (col 14 lines 21-27), and in response thereto, swaps the first primary instruction buffer with the first backup instruction buffer (col 7 line 52 to col 8 line 3); and (2) detects when the second thread stalls (col 14 lines 21-27), and in response thereto, swaps the second primary instruction buffer with the second backup instruction buffer (col 7 line 52 to col 8 line 3).

Note that, as discussed in the combination above, the third/fourth threads (second primary and backup threads) are considered to act in a similar fashion as the first and second threads.

18. Regarding claim 8, Doing/Shoemaker discloses an integrated circuit processor (col 2 lines 52-53) comprising: a first primary instruction buffer corresponding to a first primary thread (fig 2 reference 203); a second primary instruction buffer corresponding to a second primary thread (col 7 lines 55-56); wherein the first and second primary threads simultaneously issue instructions for execution; a first backup instruction buffer (col 7 lines 55-56); a second backup instruction buffer; a thread switch mechanism that detects when the first thread stalls (col 14 lines 21-27), and in response thereto, begins issuing from the first backup instruction buffer, and that detects when the second thread

stalls, and in response thereto, begins issuing from the second backup instruction buffer (col 14 lines 21-27).

Note that the distinction between the first and second primary threads do not matter, because the each primary thread are considered to be symmetric.

19. Regarding claim 14, Doing discloses the method of claim 9 further comprising the steps of: (D) providing a third instruction buffer corresponding to a third thread (fig 2 reference 203); (E) providing a fourth instruction buffer corresponding to a fourth thread (fig 2 reference 204); and (F) swapping information stored in the third instruction buffer with information stored in the fourth instruction buffer (col 7 lines 60-64).

20. Regarding claim 15, Doing discloses the method of claim 14 wherein step (F) is performed when the third thread stalls (col 14 lines 21-27).

21. Regarding claim 16, Doing discloses the method of claim 14 wherein step (F) is performed when the fourth thread stalls (col 14 lines 21-27).

22. Regarding claim 17, Doing discloses the method of claim 14 wherein the first and third threads simultaneously issue instructions for execution (Shoemaker paragraph 6).

23. Regarding claim 18, Doing discloses a method for switching between first and second threads (col 7 line 52 to col 8 line 3) of execution in a multithreaded processor

(col 5 lines 10-14), the method comprising the steps of: (A) providing a first primary instruction buffer corresponding to the first thread (fig 2 reference 203 and col 7 lines 55-56); (B) providing a second primary instruction buffer corresponding to the second thread (see claim 3); (C) providing a first backup instruction buffer corresponding to a first backup thread (fig 2 reference 204 and col 7 lines 60-64); (D) providing a second backup instruction buffer corresponding to a second backup thread; (E) simultaneously issuing instructions from the first primary instruction buffer and from the second primary instruction buffer; and (F) detecting when one of the first and second primary threads stalls (col 14 lines 21-27 and col 7 lines 60-64), and in response thereto, swapping information stored in one of the first and second primary instruction buffers corresponding to the stalled thread with information stored in one of the first and second backup instruction buffers (col 7 line 52 to col 8 line 3).

24. Regarding claim 19, Doing discloses the method of claim 18 wherein step (E) comprises the steps of: (1) detecting when the first primary thread stalls (col 14 lines 21-27), and in response thereto, swapping information stored in the first primary instruction buffer with information stored in the first backup instruction buffer (col 7 line 52 to col 8 line 3); and (2) detecting when the second thread stalls, and in response thereto, swapping information stored in the second primary instruction buffer with information stored in the second backup instruction buffer (col 7 line 52 to col 8 line 3).

25. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing/Shoemaker in view of Levy (U.S. Patent No. 6,314,511).

26. Regarding claim 7, Doing discloses the integrated circuit processor of claim 5.

Doing/Shoemaker fails to disclose a pool of backup buffers.

Levy discloses the use of a pool of registers to be used for register renaming during a context switch (col 12 lines 34-45).

Doing/Shoemaker (as previously combined) has a single backup thread for each primary thread. This technique can allow for useful processing during a cache miss; however, utilizing a technique analogous to Levy would allow for "the most flexible technique for managing" the instruction buffers (Levy col 12 lines 35-36). More flexibility for thread switching allows for better utilization of processor resources during a latency situation caused by a cache miss.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the computing system of Doing/Shoemaker to utilize a system analogous to the register renaming system of Levy in which a pool of threads can be used to backup the primary threads, rather than just a single backup option. This way, any backup instruction buffer in the pool may be swapped with information in the first primary instruction buffer and information in any backup instruction buffer in the pool may be swapped with information in the secondary primary buffer (col 12 lines 36-41).

27. Regarding claim 20, Doing/Shoemaker/Levy discloses the method of claim 18 wherein the first and second backup instruction buffers are part of a pool of backup instruction buffers (Levy col 12 lines 34-45), wherein information in any backup instruction buffer in the pool may be swapped with information in the first primary instruction buffer (col 12 lines 36-41), and wherein information in any backup instruction buffer in the pool may be swapped with information in the second primary instruction buffer (col 12 lines 36-41).

28. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing/Shoemaker in view of Redington (U.S. Patent No. 6,957,326).

29. Regarding claim 21, Doing discloses a method for switching between threads of execution in a multithreaded processor (col 7 line 52 to col 8 line 3), the method comprising the steps of: (A) providing a first primary instruction buffer corresponding to the first thread (fig 2 reference 203 and col 7 lines 55-56); (B) providing a second primary instruction buffer corresponding to the second thread (see claim 3); (C) providing a first backup instruction buffer corresponding to a first backup thread (fig 2 reference 204 and col 7 lines 60-64); (D) providing a second backup instruction buffer corresponding to a second backup thread; (E) simultaneously issuing instructions from the first primary instruction buffer and from the second primary instruction buffer (Shoemaker paragraph 6); and (F) detecting when the first threads stalls (col 14 lines 21-27).

Doing/Shoemaker fails to disclose issuing from a backup instruction buffer rather than the primary instruction buffer.

Redington discloses, during a context switch, allowing register sets to switch roles from primary to secondary and vice versa (col 4 lines 31-39).

It is expected that Doing/Shoemaker as well as others of ordinary skill appreciate the advantage of power consumption in a processor. The technique disclosed in Doing/Shoemaker of exchanging instruction information is effective, but not necessarily power efficient. For that reason, Doing/Shoemaker would be motivated to utilize a technique that required less information transfer and, therefore, less power consumption during a context switch.

It would have been obvious at the time of the invention for one of ordinary skill in the art to allow the computing system of Doing/Shoemaker to reverse the roles of the primary and secondary instruction buffers (similar to the registers disclosed in Redington) in such a way that after a thread change, instructions will be executed from the previously secondary (curently primary) instruction buffer.

30. Regarding claim 22, Doing discloses the method of claim 21 further comprising the step of (G) detecting when the second thread stalls, and in response thereto, issuing from the second backup instruction buffer instead of issuing from the second primary instruction buffer (Redington col 4 lines 31-39).

Claim Rejections - 35 USC § 102

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

31. Claim 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Luick (U.S. Publication No. 2005/0081018)

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1-20, limitations regarding changing threads in response to a cache miss are disclosed by paragraph 23.

Limitations regarding exchanging information between two instruction buffers as a result of a context switch are disclosed by paragraph 21 lines 8-14.

Limitations regarding a "pool" of backup threads are disclosed by paragraph 24 lines 4-11 and paragraph 25.

Limitations regarding an integrated circuit are disclosed in the first line of claim 1 and paragraph 6 lines 8-9.

Limitations regarding a third and forth instruction buffer are disclosed by paragraph 17.

Note that the it is assumed that the functionality of the register apply directly to instruction buffers based on paragraph 21, stating "assuming that the instruction buffers are implemented in a similar way as the register files".

Conclusion

32. The following is text cited from 37 CFR 1.11(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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